

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

THOMAS D. SIMON, ET AL.

Application No.:

Filed:

For: **Electromagnetically-Coupled BUS System**

Art Group: 2189

Examiner: Lefkowitz, Sumati

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted concurrently with the Continuation Application. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s). Some or all of the references listed on the enclosed PTO/SB/08 were previously identified in the parent application (Application No. 09/714,321, filed November 15, 2000) and copies of the references were furnished at that time. Accordingly, per 37 CFR §1.98(d)(1) additional copies of those references are not submitted herewith.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: _____

9/23/03

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Substitute for form 1449A/PTO (Modified by BSTZ 6/30/99) INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>			<i>Complete if Known</i>		
			Application Number		
			Filing Date		
			First Named Inventor		
			Group Art Unit		
Examiner Name			Not Yet Assigned		
Sheet	2	of	4	Attorney Docket Number	
			42390.P10493		


U.S. PATENT DOCUMENTS					
Examiner Initials *	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Filing Date if Appropriate
		Number			
		3,619,504	De Veer et al.	11/9/1971	12/24/1969
		6,005,895	Perino et al.	12/21/1999	12/20/1996
		5,629,838	Knight et al.	5/13/1997	6/24/1994
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FOREIGN PATENT DOCUMENTS						
Examiner Initials *	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation? Yes/No
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OTHER DOCUMENTS		
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	XTL Evaluation System Evaluation Memory Sub-System: Chip (HS-TEG: High Speed Test	
	Engineering Group) and Dimm, 9/15/2000, Pages 22-35, Volume SDL601-XTL-0-073 DMX 005	
	Systems Development Laboratory, Hitachi Ltd.,	
	HIDEKI OSAKA, High Performance Memory Interface for DDR-SDRAM II: XTL	
	(Crosstalk Transfer Logic), 9/15/2000, Pages 2-21, Volume SDL601-XTL-0-074 DMX 006	

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Examiner Name				Not Yet Assigned		
Attorney Docket Number				42390.P10493		
Sheet	3	of	4			

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	Systems Development Laboratory, Hitachi Ltd., RAMIN FARJAD-RAD, ET AL. A 0.3- μ m	
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	of Solid-State Circuits, Vol. 35, No. 5	
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	Oversampling, May 5, 1998, Pages 713-722, IEEE Journal of Solid-State Circuits, Vol. 33 No. 5	

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Notice of References Cited	Application/Control No.	Applicant(s)/Patent Under Reexamination SIMON ET AL.	
	Examiner	Art Unit	Page 4 of 4

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,496,886	12-2002	Osaka et al.	710/100
	B	US-6,449,308	09-2002	Knight et al.	375/212
	C	US-6,446,152	09-2002	Song et al.	375/371
	D	US-6,111,476	08-2000	Williamson, John Michael	333/109
	E	US-6,016,086	01-2000	Williamson et al.	333/109
	F	US-5,365,205	11-1994	Wong, Larry K.	333/109
	G	US-3,835,252	09-1974	Ananiades et al.	375/257
	H	US-3,786,418	01-1974	Nick, Howard H.	375/257
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	J	US-			
	K	US-			
	L	US-			
	M	US-			

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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